

App. No. 10/651,849
Amendment Dated: March 23, 2005
Reply to Office Action of December 23, 2004

REMARKS/ARGUMENTS

Claims 1-20 are pending in this application. The Office Action, dated December 23, 2004: rejected claims 10 -12 under 35 USC § 112, rejected claims 3-9 under 35 USC § 102(e) as being anticipated by Lauffenburger et al. (US Patent No. 6,657,487), rejected claims 1-3, 13 and 15-20 under 35 USC § 102(b) as being anticipated by Linder et al. (US Patent No. 5,581,213), rejected claims 1 and 10 under 35 USC § 102(b) as being anticipated by Sohn (US Patent No. 6,313,964), and indicated that claims 11, 12 and 14 would be allowable if appropriate corrections are made. Claim 10 is amended to correct for a minor error without any change in the scope of the subject matter that is claimed. Claims 1, 15 and 20 are amended to clarify that which the Applicant considers the invention. Claim 21 is added and it is believed that no further search is required for proper consideration. No new matter has been added.

Rejection of Claims 10 - 12 under 35 USC § 112

Claims 10 - 12 are rejected under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In specific, claim 10 lacked antecedent support for "the first node", "the second node", and included a typographical error. Also, claims 11 - 12 depend upon and further limit claim 10, and are specifically rejected for the indefiniteness of claim 10.

Claim 10 is amended to correct for the minor infelicities noted by the Examiner. Claims 11 - 12 should now also be allowable since claim 10 is now in proper form. For the reasons stated above, claims 10 - 12 are in proper form for allowance and notice to that effect is requested.

App. No. 10/651,849
Amendment Dated: March 23, 2005
Reply to Office Action of December 23, 2004

Rejection of Claims 1 - 3, 13 and 15-20 under 35 USC § 102(b)

Claims 1 - 3, 13 and 15-20 are rejected under 35 USC § 102(b) as being anticipated by Linder et al. (US Patent No. 5,581,213). The office action states:

With respect to claims 1-3, 13 and 15-19, Linder et al. discloses, in Figs. 2 and 6, a circuit comprising: "a first amplifier means (g_{m1})"; "a common node (13)"; "a second amplifier means (g_{m2})"; "a reference signal (V_L)"; "a third amplifier means (g_{m3})"; "a second stage means (12)"; "a feedback means (R_f and R_{fb})"; and "a null control means (10)", all connected and operating similarly as recited by Applicant.

Claim 1 as amended includes at least the following limitations that are not taught by the Linder reference:

"a first stage circuit that includes an array of amplifier circuits, wherein each of the amplifier circuits includes: an offset adjustment circuit ... and a null control input that is arranged to receive a respective null control signal ..."; and
"a null control logic circuit ... arranged ... such that the amplifier circuits are selectively zeroed to minimize the effects of offset in each of the amplifier circuits.."

Nothing in the Linder reference teaches the use of an offset adjustment circuit and a null control logic circuit as is described in Applicant's claim 1. As described in the Linder reference at col 3, line 19, "[t]he unique aspect of the invention is the provision of a variable resistor circuit 6, whose resistance R_g can be controlled through a control voltage terminal V_C ...". As described in the Linder reference at col. 4, line 23, "The components of the variable resistance circuit 6 ... are disclosed ... as part of a variable gain amplifier circuit." At col. 4, line 34, the Linder reference described that "The control circuit 10 determines which of the gm stages are activated ...". As a whole, the Linder reference teaches to adjust the gain of a variable gain amplifier by adjusting an amount of resistance (R_b) by selectively activating gm stages.

App. No. 10/651,849
Amendment Dated: March 23, 2005
Reply to Office Action of December 23, 2004

However, nothing in the Linder reference describes an offset adjustment circuit, an offset voltage associated with an amplifier, nor a null control means as is described in Applicants claim 1.

Claim 15 as amended includes at least the following limitations that are not taught by the Linder reference:

"a first amplifier means that includes a first offset adjustment circuit ...";
"a second amplifier means that includes a second offset adjustment circuit ...";
"a third amplifier means that includes a third offset adjustment circuit";
and
"a null control means ... such that an offset voltage ... is selectively zeroed..."

For at least the reasons stated previously with respect to claim 1, nothing in the Linder reference teaches the use of offset adjustment circuits and a null control means as is taught by applicant's claim 15.

Claim 20 as amended includes at least the following limitations that are not taught by the Linder reference:

"... each of the amplifier circuits includes an offset adjustment circuit therein;"
"selecting one of the array of amplifier circuits for offline operation;"
"nulling an offset voltage associated with the selected amplifier circuit while the selected amplifier circuit is in offline operation;" and
"maintaining the non-selected amplifier circuits such that the offset voltage associated with the reference signal is zeroed as an average."

For at least the reasons stated previously with respect to claims 1 and 15, nothing in the Linder reference teaches the use of offset adjustment circuits, selecting an amplifier circuit for

App. No. 10/651,849
Amendment Dated: March 23, 2005
Reply to Office Action of December 23, 2004

offline operation, nulling the selected amplifier circuit for offset voltage, and maintaining the non-selected amplifier circuits as is taught by applicant's claim 20.

For those reasons described above, claims 1, 15, and 20 are believed to be allowable. Claims 2-3 and 13 depend upon and further limit claim 1, and should be allowable for that reasons as well as any additional limitations they recite. Claims 16-19 depend upon and further limit claim 15, and should be allowable for that reason as well as any additional limitations they recite. Claims 1-3, 13, and 15-20 are believed to be in proper form for allowance and notice to that effect is requested.

Rejection of Claims 1 and 10 under 35 USC § 102(b)

Claims 1 and 10 are rejected under 35 USC § 102(b) as being anticipated by Sohn (US Patent No. 6,313,964). The office action states:

Sohn discloses, in Fig. 6, a circuit comprising: "a first stage means that includes an array of amplifier circuit (10 and 12)"; "a common node (providing VG)"; "a second stage means (14)"; "a reference signal (VINT)"; "a feedback means (lines connecting VINT to N2 and N6)"; and "a null control means (providing CSIVC)", wherein at least one of the amplifier circuits includes "a first transistor (N1)", "a second transistor (N2)", "a third transistor (P2)", "a fourth transistor (P1)" and "a fifth transistor (N3 and/or N4), all connected and operating similarly as recited by Applicant.

Claim 1 as amended includes at least the following limitations that are not taught by the Sohn reference:

"a first stage circuit that includes an array of amplifier circuits, wherein each of the amplifier circuits includes: an offset adjustment circuit ... and a null control input that is arranged to receive a respective null control signal ..."; and "a null control logic circuit ... arranged ... such that the amplifier circuits are selectively zeroed to minimize the effects of offset in each of the amplifier circuits.."

App. No. 10/651,849
Amendment Dated: March 23, 2005
Reply to Office Action of December 23, 2004

Nothing in the Sohn reference teaches the use of an offset adjustment circuit and a null control logic circuit as is described in Applicant's claim 1. The Sohn reference describes that a normal operating mode is active when the CSVTVC control signal is high, and the standby mode is active when the CSVTVC control signal is low. As described in the Sohn reference at col. 4, line 9, "the transistors in the differential comparison circuit 10 and output driver 14 for active mode are larger ... than those used in the differential comparison circuit 12 and output driver 16 for standby mode, thereby resulting in larger current drive capacity."

As a whole, the Sohn reference teaches to use two differential comparison circuits with different size devices so that you can minimize current consumption and increase signal drive when high current output is necessary. However, nothing in the Sohn reference describes an offset adjustment circuit, an offset voltage associated with an amplifier, nor a null control means as is described in Applicants claim 1. Claim 1 is believed to be allowable. Claim 10 depends upon and further limits claim 1. For at least those reasons discussed above, claims 1 and 10 are believed to be in proper form for allowance and notice to that effect is requested.

Rejection of Claims 3 - 9 under 35 USC § 102(e)

Claims 3-9 are rejected under 35 USC § 102(e) as being anticipated by Lauffenburger et al. (US Patent No. 6,657,487). The office action states:

Lauffenberger discloses, in Figs. 2 and 3, a circuit comprising: "a first stage means (32) that includes an array of amplifier circuits"; "a common node (outputs of switches 48-64)"; "a second stage means (68)"; "a reference signal (output of Gm)"; "a feedback means (72)"; and "a null control means (34)", all connected and operating similarly as recited by Applicant.

App. No. 10/651,849
Amendment Dated: March 23, 2005
Reply to Office Action of December 23, 2004

Claim 3-9 depend upon and further limits claim 1. Claim 1 as amended includes at least the following limitations that are not taught by the Lauffenberger reference:

"a first stage circuit that includes an array of amplifier circuits, wherein each of the amplifier circuits includes: an offset adjustment circuit ... and a null control input that is arranged to receive a respective null control signal ..."; and

"a null control logic circuit ... arranged ... such that the amplifier circuits are selectively zeroed to minimize the effects of offset in each of the amplifier circuits.."

Nothing in the Lauffenberger reference teaches the use of an offset adjustment circuit that is located with the array of amplifier circuit, and a null control logic circuit that are arranged to cooperate with one another as is described in Applicant's claim 1. Moreover, it is unclear how claims 3 - 9 are anticipated by the Lauffenberger reference in that, the office action is silent as to the specific structural limitations that are found in applicant's claims 3 - 9 and offers little guidance as to Lauffenburger providing such specific structural features. Claims 3 - 9 depend upon and further limit claim 1 which is proposed to be allowable for those reasons described above. Claims 3 - 9 are proposed to be allowable and notice to that effect is respectfully requested.

App. No. 10/651,849
Amendment Dated: March 23, 2005
Reply to Office Action of December 23, 2004

In view of the foregoing amendments and remarks, all pending claims are believed to be allowable and the application is in condition for allowance. Therefore, a Notice of Allowance is respectfully requested. Should the Examiner have any further issues regarding this application, the Examiner is requested to contact the undersigned attorney for the applicant at the telephone number provided below.

Respectfully submitted,

MERCHANT & GOULD P.C.


Brett A. Hertzberg
Registration No. 42,660
Direct Dial: 206.342.6255

MERCHANT & GOULD P.C.
P. O. Box 2903
Minneapolis, Minnesota 55402-0903
206.342.6200
BAH/ab

